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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,452	10/17/2001	Manjunath D. Hiritsa	SUN-P5403	7441

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EXAMINER	
TAT, BINH C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/982,452	HARITSA ET AL.	
	Examiner	Art Unit	
	Binh C. Tat	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-77* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-77* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicants' Amendment and Response to Final Office Action has been examined. The specification and drawings are amended. Claims 1-77 remain pending in the application.

Continued Examination Under 37 CFR 1.114

1. A Request for Continued Examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 17 May 2004 has been entered.

Terminal Disclaimer

2. The terminal disclaimer filed on 17 May 2004 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of any patent granted on application 09/982,459 filed on 17 October 2001 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-77 are rejected under 35 U.S.C. 102(e) as being anticipated by Camporeses et al. (U.S Patent 6205571).

4. As to claim 1 (method), 16 (apparatus), 31 (apparatus), and 43 (computer readable medium), Camporeses et al. teaches a method of determining clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising: partitioning the complete clock net into a global clock net and a plurality of local clock nets (see fig 2, 4, and 5 element 201 col 4 lines 20-40); simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, said simulating including measuring clock arrival time and slope at each point where a clock element is connected (see fig 7 col 6 lines 10 to col 9 lines 60); simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets (see fig 7 col 11 lines 34 to col 12 lines 26); and combining the plurality of simulations to form a complete clock net simulation (see fig 7 col 11 lines 34 to col 12 lines 26).

5. As to claims 2, 17, 32 and 44, Camporeses et al. teaches wherein partitioning comprises breaking the complete clock net into a plurality of parts approximating rectangular grid coordinates (see fig 2, 4, and 5).

6. As to claims 3, 18, 33, and 45 Camporeses et al. teaches further comprising breaking at least one of the plurality of local clock nets down into at least one sub-local clock net (see fig 2, 4, and 5 element 201 col 4 lines 20-40).

7. As to claim 4, 19, 34 and 46, Camporeses et al. teaches further comprising simulating the at least one sub-local clock net prior to simulating the corresponding local clock net (see fig 7 col 9 lines 8-65).

8. As to claims 5, 20, 35, and 47, Camporeses et al. teaches wherein at least two of the plurality of local clock nets are simulated in parallel (see fig 7 col 9 lines 8-65).

9. As to claims 6, 21, 36, and 48, Camporeses et al. teaches wherein simulating each of the plurality of local clock nets comprises: extracting a layout of the local clock net and the conductors routed above and through the local clock net from a microprocessor network database (see fig 7 col 6 lines 10-65); extracting component values of the elements of the local clock net from the microprocessor network database (see fig 7 col 6 lines 10-65); simulating the local clock net based on the layout and the component values (see fig 7 col 6 lines 10-65); and extracting a load of the local clock net on the global clock net (see fig 7 col 6 lines 10-65).

10. As to claims 7, 22, 37, and 49, Camporeses et al. teaches wherein simulating the local clock net comprises assuming that the clock arrival times from the global clock net will be simultaneous at all points where the local clock net is connected to the global clock net (see fig 7 col 9 lines 8-65).

11. As to claims 8, 23, 38, and 50, Camporeses et al. teaches wherein simulating the global clock net comprises: extracting the layout of the global clock net from a microprocessor network database (see fig 7 col 6 lines 10-65); extracting component values of the elements of the global clock net from the microprocessor network database (see fig 7 col 6 lines 10-65); inserting the simulated loads of the plurality of local clock nets (see fig 7 col 6 lines 10-65); and simulating the global clock net based on the layout, the component values, and the simulated local clock net loads (see fig 7 col 6 lines 10-65).

12. As to claims 9, 24, 39, and 51, Camporeses et al. teaches further comprising storing the plurality of simulation results in a Clock Data Model (see fig 2 col 3 line 40-60).

13. As to claims 10, 25, 40, and 52, Camporeses et al. teaches further comprising evaluating the complete clock net to determine whether the results converge (see fig 7 col 9 lines 8-65).

14. As to claims 11, 26, 41, and 53, Camporeses et al. teaches wherein, if the results do not converge, the method further comprises: assuming that clock arrival times are those calculated for the simulated global clock net (see fig 7 col 9 lines 8-65); re-simulating at least one of the plurality of local clock nets to generate a load for the at least one local clock net on the global clock net (see fig 7 col 11 lines 34 to col 12 lines 26); re-simulating the global clock net based in part on the simulated or re-simulated load of each of the plurality of local clock nets (see fig 7 col 11 lines 34 to col 12 lines 26); and combining the simulations and re-simulations to form the complete clock net (see fig 7 col 11 lines 34 to col 12 lines 26).

15. As to claims 12, 27, and 54, Camporeses et al. teaches wherein re-simulating at least one of the plurality of local clock nets comprises: re-simulating the at least one local clock net based on the layout, the component values, and the calculated clock arrival times (see fig 7 col 11 lines 34 to col 12 lines 26); and extracting a load of the at least one local clock net on the global clock net (see fig 7 col 11 lines 34 to col 12 lines 26).

16. As to claims 13, 28, and 55, Camporeses et al. teaches further comprising re-simulating at least a second of the plurality of local clock nets in parallel with the at least one local clock net (see fig 7 col 6 lines 10-65).

17. As to claims 14, 29, and 56, Camporeses et al. teaches wherein re-simulating the global clock net comprises: inserting the simulated or re-simulated loads of the plurality of local clock nets (see fig 7 col 6 lines 10-65); and re-simulating the global clock net based on the layout, the component values, and the simulated or re-simulated local clock net loads (see fig 7 col 6 lines 10-65).

18. As to claims 15, 30, 42, and 57, Camporeses et al. teaches further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model (see fig 7 col 11 lines 34 to col 12 lines 26).

19. As to claims 58 (method), 63 (apparatus), 68 (apparatus), and 733 (computer readable medium), Camporeses et al. teaches a method of determining and analyzing clock insertion delays for a microprocessor design having grid-based clock distribution, the method comprising: partitioning the complete clock net into a global clock net and a plurality of local clock nets (see fig 2, 4, and 5 element 201 col 4 lines 20-40); simulating each of the plurality of local clock nets to generate a load for each of the plurality of local clock nets on the global clock net, said simulating including measuring clock arrival time and slope at each point where a clock element is connected (see fig 7 col 6 lines 10 to col 9 lines 60); simulating the global clock net based in part on the simulated load of each of the plurality of local clock nets (see fig 7 col 11 lines 34 to col 12 lines 26); combining the plurality of simulations to form complete clock net simulation (see fig 7 col 11 lines 34 to col 12 lines 26); and analyzing the complete clock net to predict the clock skew for a given data transfer path (see fig 7 col 11 lines 34 to col 12 lines 26).

20. As to claims 59, 64, 69, and 74, Camporeses et al. teaches wherein analyzing comprises: adjusting an insertion delay of the involved elements of the given data transfer

path (see fig 7 col 11 lines 34 to col 12 lines 26); and re simulating at least one local clock net involved in the given data transfer path (see fig 7 col 11 lines 34 to col 12 lines 26).

21. As to claims 60, 65, 70, and 75, Camporeses et al. teaches further comprising, when the at least one re-simulated local clock net is connected to at least one sub-local clock net, evaluating the clock arrival times to determine whether the sub-local clock net should be re-simulated (see fig 7 col 6 lines 10 to col 9 lines 60).

22. As to claims 61, 66, 71, and 76, Camporeses et al. teaches further comprising evaluating the at least one re-simulated clock net load to determine whether at least one higher clock net connected to the at least one re-simulated local clock net should be re-simulated (see fig 7 col 6 lines 10 to col 9 lines 60).

23. As to claims 62, 67, 72, and 77, Camporeses et al. teaches further comprising storing the plurality of simulation and re-simulation results in a Clock Data Model (see fig 7 col 11 lines 34 to col 12 lines 26).

Remarks

In this continued examination, Applicants attempt to distinguish Camporese by inserting the limitations reciting *measuring clock arrival time and slope and each point where a clock element is connected.* However, Camporese discloses measuring arrival times at grid intersection points and it is well known in the art that delay times are based on the slope of input transitions (see fig 7 col 6 lines 10 to col 9 lines 60).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (703) 305-4855. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

VUTHE SIEK
PRIMARY EXAMINER

Binh Tat
Art Unit 2825
August 20, 2004